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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,439	JEDDELOH, JOSEPH	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-12, 14-16, 18-26, 28-39, and 40-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,914,727 to Horan et al. and U.S. Patent No. 5,860,101 to Arimilli et al.

3. As per claim 1, Horan teaches a computer system comprising: a first of the at least two memory controllers (Fig. 3 and c. 11 ll. 5-18: *core logic chipset 204 functionally comprises memory interface and control 304*) is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory (Fig. 2 and c. 10 ll. 47-54: *core logic chipset 204 connected to the host bus 103, PCI bus 109, and memory bus 105*), and also wherein the first of the at least two memory controllers comprises an accelerated graphics port for establishing a dedicated point-to-point connection between the first of the at least two memory controllers and an accelerated graphics processor (Fig. 2 and c. 10 ll. 50-51: *core logic chipset 204 connected to the graphics controller through an AGP bus 207*).

4. Horan discloses that multiple CPUs in a symmetric or asymmetric multi-processor configuration are contemplated and within the scope of the present invention (c. 10 ll. 45-46 and c. 11 ll. 16-18), but does not expressly teach at least two memory controllers for controlling a main memory. Arimilli teaches a symmetric multiprocessor system comprising multiple partial

system memories 18a-18n and corresponding memory controllers 17a-17n (Fig. 2 and c. 6 ll. 18-22) providing the benefit of scalability and parallel bus traffic between the memory controller and system memory. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combined the teachings of Horan and Arimilli whereby the symmetric multiprocessor system contemplated by Horan is implemented with multiple memory controllers and associated system memory as taught by Arimilli in order to provide the benefits of scalability and parallel bus traffic between the memory controller and system memory.

5. As per claim 2, Horan discloses: wherein the first of the at least two memory controllers defines a range of addresses in memory that are preferentially used over other addresses for storage of graphics data for transactions associated with the dedicated point-to-point connection (c. 18 ll. 65-c. 19 ll. 4 and Figs. 16 and 17A: *chipset configuration registers implemented in the host to PCI bridge function, including register 1702*; *A Base Address Register 0, BAR0, is used to allocate AGP device address space for the AGP compliant master*).

6. As per claim 4, Horan discloses: wherein the first of the at least two memory controllers maintains a graphical address remapping table comprising at least one page table entry (PTE) providing information for translation of a virtual address to a physical address (c. 9 ll. 51-59: *The core logic chipset utilizes a graphics address remapping table to remap virtual addresses to physical addresses of graphics information located in the system memory*), wherein the virtual address includes a first portion and a second portion (Fig. 7: *graphics controller device address comprising page offset from AGP base address portion and offset into 4KB page portion*), the first portion corresponding to a PTE in the graphical address remapping table (Fig. 9: *page offset from AGP base address corresponding to address of GART entry*) and wherein the second

portion and information provided by the PTE are combined to provide the physical address (Fig. 9: *offset into 4KB page portion of the graphics controller device address combined with address of GART entry yields the physical address*).

7. As per claim 5, Horan discloses, wherein the first portion comprises a virtual page number field (Fig. 9: *page offset from AGP base address*).

8. As per claim 6, Horan discloses, wherein the second portion comprises an offset field (Fig. 9: *offset into 4KB page*).

9. As per claim 7, Horan discloses wherein the graphical address remapping table is configured by loading at least one configuration register during boot up of a computer system (c. 27 ll. 1-5 and ll. 30-35: *During boot, system BIOS power-on self-test configures the core logic chipset with size of AGP device address space*).

10. As per claim 8, Horan discloses additionally comprising one configuration register includes a starting address of the graphical address remapping table (c. 22 ll. 16-18: *A GART Table/Directory Base Address Register 1910 provides the physical address for the GART table/directory in system memory*).

11. As per claim 9, Horan discloses wherein the at least one configuration register includes a boundary address defining the lowest address of a graphical address remapping table range (c. 22 ll. 16-18: *GART Table/Directory Base Address Register 1910 provides the physical address for the GART table/directory in system memory*).

12. As per claim 10, Horan discloses wherein the at least one configuration register includes a range register defining the amount of memory that is preferentially used over other addresses for storage of graphics data for accelerated graphic port transactions (c. 21 ll. 42-44: *An AGP*

Device Address Space Size Register 1828 determines the size of AGP Device Address Space to be allocated by system BIOS).

13. As per claim 11, Horan discloses wherein an initialization BIOS loads the at least one configuration register (c. 27 ll. 1-5 and ll. 30-35: *During boot, system BIOS power-on self-test configures the core logic chipset with size of AGP device address space*).

14. As per claim 12, Horan discloses wherein an operating system API loads the at least one configuration register (c. 26 ll. 57-59: *Key components of the AGP software architecture include System BIOS, the chipset miniport driver, the operating system, and the graphics or Direct Draw driver. These components are required to initialize and control the AGP and GART table functions within the chipset and graphics controller*).

15. Claims 14, 15, and 18-26 are similar in scope to claims 1, 2, and 4-12, and are rejected under the same rationale.

16. As per claim 16, Horan does not expressly teach at least two of the at least two memory controllers include an accelerated graphics port. Horan contemplates a symmetric or asymmetric multi-processor configuration as within the scope of his invention (c. 10 ll. 45-46 and c. 11 ll. 16-18), and Arimilli teaches a symmetric multiprocessor system comprising multiple partial system memories 18a-18n and corresponding memory controllers 17a-17n (Fig. 2 and c. 6 ll. 18-22). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combined the teachings of Horan and Arimilli whereby the symmetric multiprocessor system contemplated by Horan is implemented with multiple memory controllers and associated system memory as taught by Arimilli wherein at least two of the memory controllers are connected to respective graphics controllers through respective AGPs in order to provide the

benefits of scalability and parallel bus traffic between the memory controller and system memory on behalf of the graphics controllers.

17. Claims 28-39 and 40-49 are similar in scope to claims 1, 2, and 4-12, and are rejected under the same rationale.

18. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,914,727 to Horan et al. and U.S. Patent No. 5,860,101 to Arimilli et al and U.S. Patent No. 6,002,411 to Dye.

19. As per claims 3 and 17, Horan does not expressly teach that at least two of the at least two memory controllers are manufactured on the same chip. Dye teaches an integrated memory controller comprising a single chip and including two memory control units for providing interface signals to communicate with respective banks of the system memory (c. 12 ll. 44-45 and c. 16 ll. 45-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Horan, Arimilli, and Dye, whereby, Horan's chipset is implemented to integrate plural memory controllers as taught by Dye in order to provide faster memory accesses through integration.

20. Claims 13 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,914,727 to Horan et al. and U.S. Patent No. 5,860,101 to Arimilli et al and U.S. Patent No. 6,118,462 to Margulis.

21. As per claims 13 and 27, Horan does not expressly teach that one of the at least two memory controllers and a memory are on a single semiconductor chip. Margulis teaches an enhanced system controller 310 connected to an input/output bridge 312, display output devices 330, a PCI bus 332, an accelerated graphics port (AGP) 334, a high-speed serial I/O port 336 (c.

4 ll. 16-19). Integrated into the enhanced system controller are additional internal memory subsystems, each with their own control and data channels (c. 4 ll. 19-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Horan and Arimilli and Margulis, and to have integrated memory with the memory controller on the chipset in order to improve memory accesses through integration.

22. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,914,727 to Horan et al. and U.S. Patent No. 5,860,101 to Arimilli et al and U.S. Patent No. 6,118,462 to Margulis and U.S. Patent No. 6,002,411 to Dye.

23. As per claim 50, Horan does not expressly teach manufacturing said at least two memory controllers and a memory on a single semiconductor chip. Margulis teaches an enhanced system controller 310 connected to an input/output bridge 312, display output devices 330, a PCI bus 332, an accelerated graphics port (AGP) 334, a high-speed serial I/O port 336 (c. 4 ll. 16-19). Integrated into the enhanced system controller are additional internal memory subsystems, each with their own control and data channels (c. 4 ll. 19-21). Dye teaches an integrated memory controller comprising a single chip and including two memory control units for providing interface signals to communicate with respective banks of the system memory (c. 12 ll. 44-45 and c. 16 ll. 45-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Horan, Arimilli, Margulis, and Dye, whereby, Horan's chipset is implemented to integrate plural memory controllers and memory as taught by Margulis and Dye in order to provide faster memory accesses through integration.

Response to Arguments

24. Applicant's arguments filed 12/27/04 have been fully considered but they are not persuasive. With respect to the claims, Applicant argues that there is no suggestion of a need in Horan to improve the scalability and parallel bus traffic between the core logic and the system RAM, and that Arimilli does not describe the usage of AGP devices and memory controllers for supporting same. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine the references is found in Arimilli and in the knowledge generally available to one of ordinary skill in the art. Arimilli recognized that it is imperial to have an expandable data-processing system that can meet all the ever-growing computing demands, and consequently, it would be desirable to provide an improved SMP data-processing system architecture such that the entire system is truly scalable (c. 1 ll. 49-57). Therefore, Arimilli provides the motivation to improve scalability in a symmetric multiprocessor system. Horan contemplates multiple CPUs in a symmetric or asymmetric multi-processor configuration as within the scope of the invention (c. 10 ll. 45-46 and c. 11 ll. 16-18). Therefore, based on Arimilli's disclosure that it is desirable to improve the scalability in a symmetric multiprocessor system, one of ordinary skill in the art would be motivated to improve the scalability in Horan's invention.

25. Applicant further argues that if the memory controller 17 of Arimilli was incorporated into the central processing unit 102 of Horan, the memory controller would be connected to a single bus, and would not be directly connected to the central processing unit bus and a bus supporting a peripheral device, as claimed. Horan teaches that the core logic chipset 204 functionally comprises memory interface and control 304, and is connected to the host bus 103, PCI bus 109, and memory bus 105 (Figs. 2 & 3, c. 10 ll. 47-54 and c. 11 ll. 5-18). Therefore, Horan teaches that a first of the at least two memory controllers is directly connected to a central processing unit bus, a bus supporting a peripheral device, and the main memory. The rejection does not suggest incorporating Arimilli's memory controller into the Horan's CPU.

Conclusion

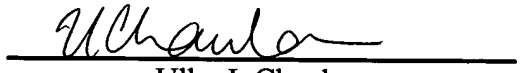
26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ulka J. Chauhan
Primary Examiner
Art Unit 2676

April 22, 2005